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Introduction

- Users of HW Performance Monitoring
- HW Performance Monitoring Tools
 - Sun's Profiling Tools
 - Application and Kernel
 - Sun's Monitoring Tools
 - Application, System, and Kernel
 - HW Counter Libraries and APIs
- HW Counter Requirements



Users and their Objectives

- Users various types
 - End users
 - End user developers
 - ISV developers
 - Compiler writers
 - Field engineers and system tuners
 - System SW developers
 - Chip designers
- Objectives for all:
 - What can I change to make things faster?



End User Tools

- Monitoring Tools
 - Both application and system
 - General overview of behavior
 - Curiosity, more than anything else:
 - End Users have few knobs to turn
 - Can change configurations:
 - Memory
 - Processors
 - Disk controllers
 - Domain partitioning
 - Application migration



End User Developer Tools

- Monitoring tools
 - Show a quick overview, system performance
 - Get data on what to profile
- Profiling Tools
 - Memory Performance: Cache, TLB
 - vs. Functions/source-lines/instructions
 - vs. Data types
 - vs. Cachelines, memory buses, controllers, pages, ...
 - Floating-point Performance
 - Report data against user's programming model
- Library APIs
 - To instrument code regions



ISV Developer Tools

- Very much like end user developers
 - But less likely to use library APIs



Compiler Writer Tools

- Monitoring and profiling
 - Compiler itself
 - Compiler-generated code
- Generated instrumentation
 - Using APIs
- Feedback-directed optimization
 - Memory profiling to inform better layout, striding
 - Branch-mispredict profiles
 - Other opportunities?



Field Engineer/System Tuner Tools

- Monitoring and profiling
 - Both user applications and system
 - Configuration management (like end users)
 - Memory
 - Processors
 - Disk controllers
 - Domain partitioning



System SW Developer Tools

- System-monitoring tools
 - Observability into OS
- Kernel profiling tools
- Runtime monitoring
 - Data to support page placement and migration
 - Understand scheduling
 - Particularly on CMT systems
- Issue: conflict with other uses of HW
 - System-level tools lock out user-level tools



Chip-designer Tools

- Not too much interest in current chips
 - Care about long-term development
 - Sometimes exploit tools on existing systems to inform next-generation designs
 - Long design cycles make this problematicLeapfrog?
 - Mostly use simulators, not old-generation chips
 - Do use current HW monitoring to validate traces
- Unanswerable questions =>
 - Better HW monitoring in next chip to get answers
 - Or so we hope



Sun's Profiling Tools

- Application profilers
 - Sun Studio—collect /Analyzer
- Kernel profilers
 - Sun Studio—er_kernel/Analyzer

- No multiplexing of HW counters
 - Hard to get valid statistics with multiplexing
 - Implies multiple runs
 - If more counters of interest than counter registers

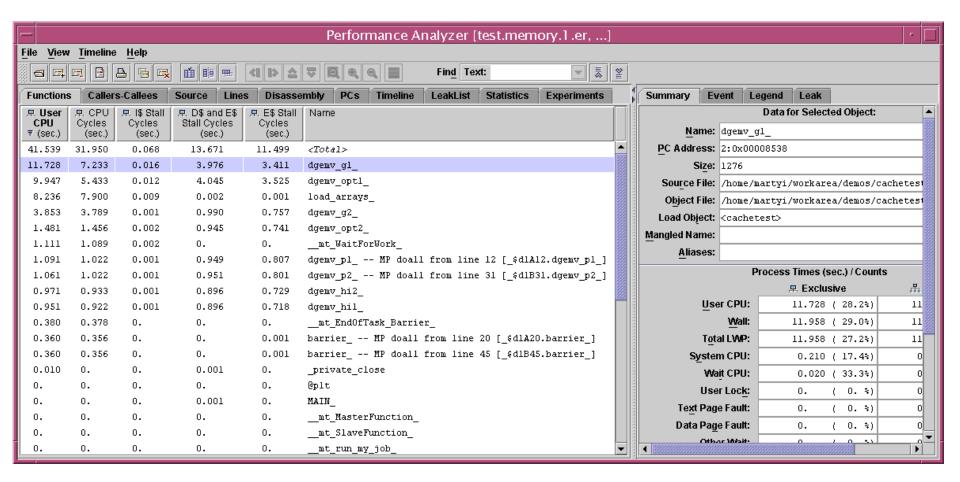


collect/analyzer

- collect -h <ctr>,<interval>, ...
 - As many counters as the HW allows
 - Automagic register assignment
- Memory counters
 - Prefix with + to record actual instruction, VA, PA
 - US-III,IV
 - Counter skid => backtracking to get data, which may fail
 - Newer chips will fix that
- Can record multiple experiments
 - Aggregate them for presentation
 - In lieu of multiplexing

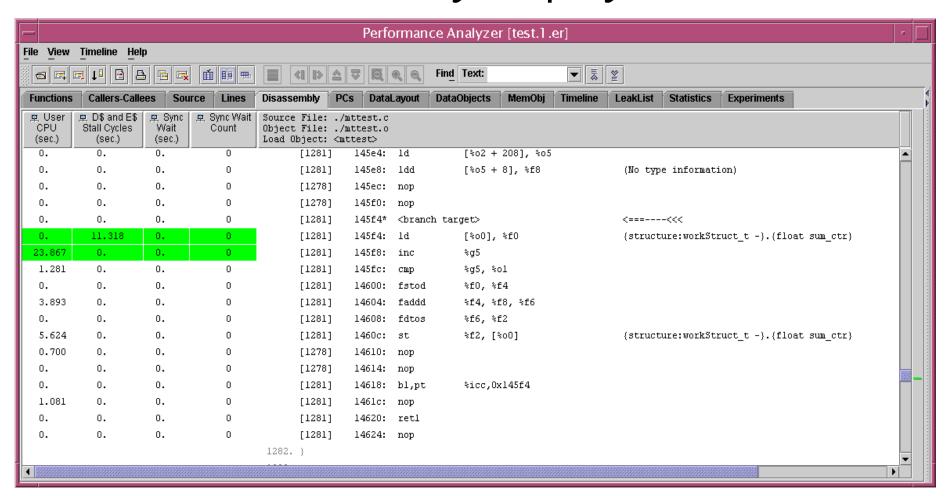


Memory Performance Profiling



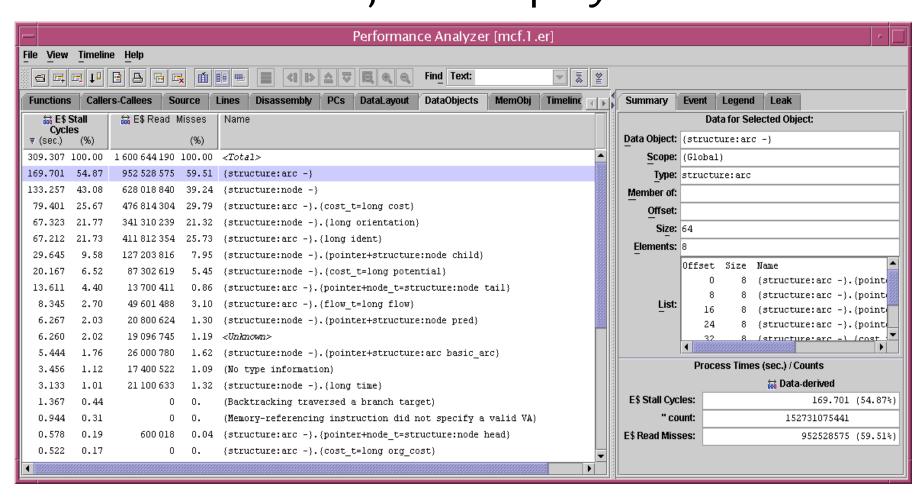


Disassembly Display



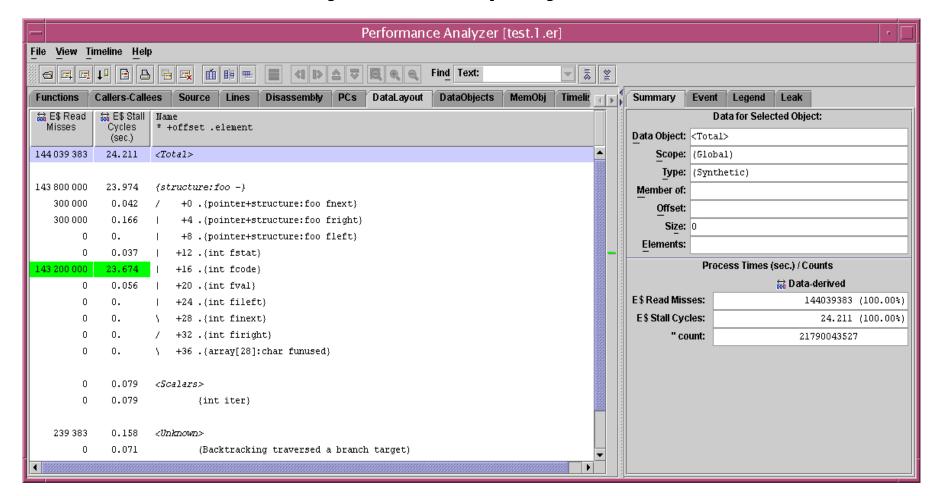


Application Profiling-Analyzer Data Objects Display



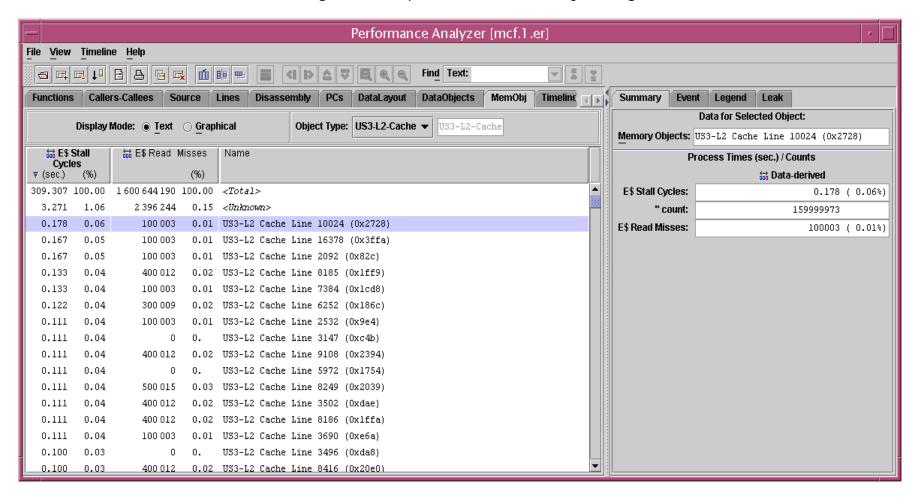


Data Layout Display



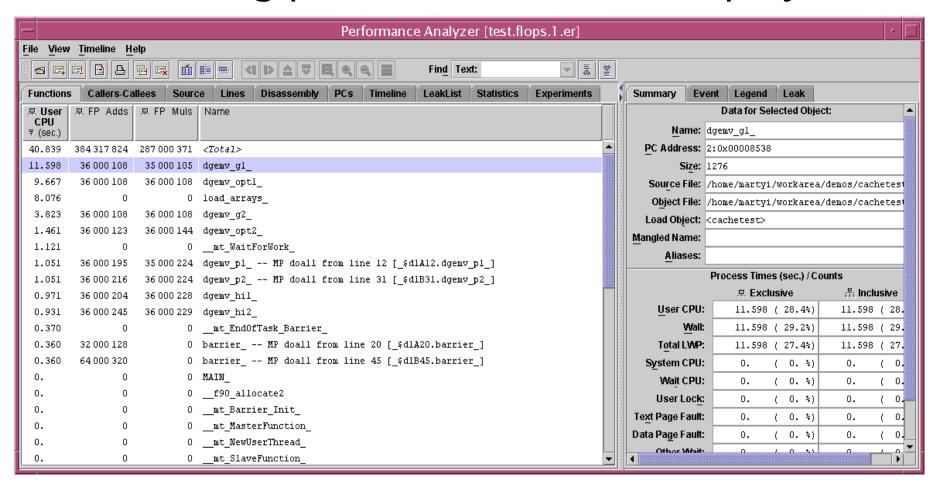


Memory Objects Display



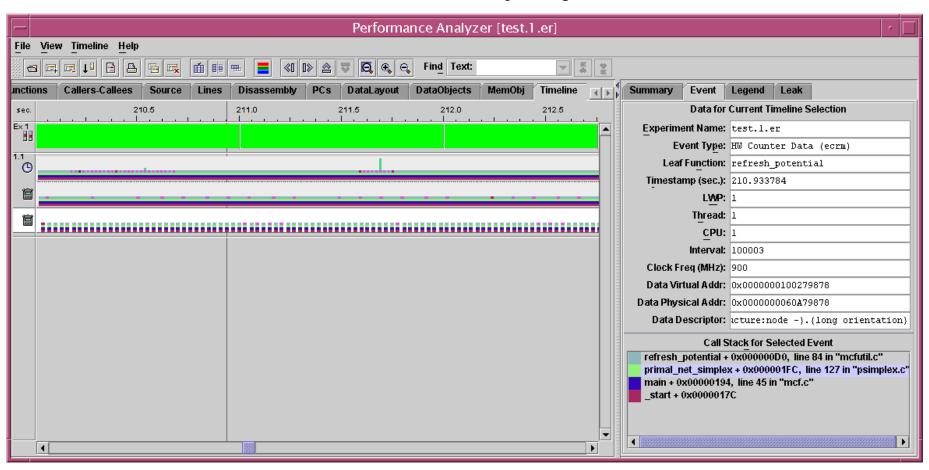


Floating-point Performance Display





Timeline Display





Kernel Profiling-Analyzer

- Similar invocation to collect
 - Can use loadable driver (internal tool)
 - For clock- or HWC-profiling
 - Use DTrace (Solaris 10)
 - Clock-profiling now
 - HWC-profiling coming
- Experiment read with Analyzer
 - Same as user profiling
- Can record simultaneous user/kernel



Sun's Monitoring Tools

- Application monitoring tools
 - cputrack
 - ripc2 (built on top of cputrack) (internal tool)
 - **bw** (internal tool)
- System monitoring tools
 - o cpustat
 - o busstat
- Allow/exploit multiplexing of HW counters
 - Valid statistics much more likely than for profiling
 - Use to see which counters to profile against



Application Monitoring-quark quarkoutput — periodic, multiplexed

```
0.103
       11100
                        tick 117322342
                                            16629 # picU=Cycle cnt,pic1=DTLB miss,sys
0.206
                                         29285156 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
       11100
                        tick
                             59287053
0.304
      11100
                                544973
                        tick
                                          5320111 # pic0=Dispatch0 IC miss,pic1=Re EC miss,sys
0.403 11100
                        tick
                                259749
                                                8 # pic0=Dispatch0 br target,pic1=Re PC miss,sys
0.503
      11100
                                 97217
                                           452879 # pic0=Dispatch0_2nd_br,pic1=Dispatch0_mispred,sys
                        tick
0.603
       11100
                        tick
                                396249
                                          2962149 # pic0=Dispatch rs mispred, pic1=Re RAW miss, sys
0.703
       11100
                        tick 79686301
                                             5287 # pic0=Rstall_storeQ,pic1=Rstall_FP_use,sys
0.872
       11100
                        tick
                               3100459
                                               18 # pic0=Rstall_IU_use,pic1=Re_FPU_bypass,sys
0.932 11100
                        tick 67885860
                                              176 # pic0=Cycle cnt,pic1=DTLB miss,sys
1.052
       11100
                        tick 148401091
                                          2241460 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
1.112
       11100
                        tick
                                  62640
                                          131944 # pic0=Dispatch0_IC_miss,pic1=Re_EC_miss,sys
                                             8 # pic0=Dispatch0_br_target,pic1=Re_FC_miss,sys
2989 # pic0=Dispatch0_2nd_br,pic1=Dispatch0_mispred,sys
1.222
       11100
                                    359
                        tick
1.352
       11100
                        tick
                                   180
1.412
       11100
                        tick
                                    633
                                            89865 # pic0=Dispatch_rs_mispred,pic1=Re_RAW_miss,sys
1.532
       11100
                                297242
                        tick
                                         35764030 # pic0=Rstall storeQ,pic1=Rstall FP use,sys
1.612
       11100
                               1359398
                        tick
                                                  # pic0=Rstall_IU_use,pic1=Re_FPU_bypass,sys
1.712
       11100
                        tick 116030624
                                               20 # pic0=Cycle cnt,pic1=DTLB miss,sys
1.832
       11100
                        tick 150258502
                                          7114364 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
1.922
       11100
                                 44256
                        tick
                                          3965119  # pic0=Dispatch0 IC miss,pic1=Re EC miss,sys
                                                4 # pic0=Dispatch0_br_target,pic1=Re_PC_miss,sys
2.032
       11100
                        tick
                                 16478
2.132
       11100
                        tick
                                   3102
                                            32512 # pic0=Dispatch0_2nd_br,pic1=Dispatch0_mispred,sys
                                             3160 # pic0=Dispatch_rs_mispred,pic1=Re RAW miss,sys
2.212
       11100
                                  1843
                        tick
2.342
                                          1659570 # pic0=Rstall_storeQ,pic1=Rstall_FP_use,sys
       11100
                                 15692
                        tick
2.492
       11100
                        tick
                                128468
                                                  # pic0=Rstall_IU_use,pic1=Re_FPU_bypass,sys
2.522
       11100
                        tick 32731512
                                               43 # pic0=Cycle cnt,pic1=DTLB miss,sys
2.612
       11100
                        tick 134166672
                                         26865067 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
2.732
       11100
                        tick
                                 75839
                                          4082663 # pic0=Dispatch0_IC_miss,pic1=Re_EC_miss,sys
2.822
       11100
                        tick
                                 14306
                                                6 # pic0=Dispatch0 br target.pic1=Re PC miss.sys
2.912
       11100
                                   2664
                                            29214 # pic0=Dispatch0 2nd br.pic1=Dispatch0 mispred.sys
                        tick
3.062
       11100
                        tick
                                  1691
                                            16143 # pic0=Dispatch rs mispred,pic1=Re RAW miss,sys
3.122
       11100
                                 10685
                                           738362 # pic0=Rstall_storeQ,pic1=Rstall_FP_use,sys
                        tick
3.212
                                                  # picO=Rstall_IU_use,pic1=Re_FPU_bypass,sys
       11100
                                102127
                        tick
3.342
       11100
                        tick 152910322
                                               68 # pic0=Cycle_cnt,pic1=DTLB_miss,sys
3.452
       11100
                        tick 166866481
                                         31695212 # pic0=Instr cnt,pic1=Re DC miss,sys
3.512
       11100
                                          2928255 # pic0=Dispatch0_IC_miss,pic1=Re_EC_miss,sys
                        tick
                                 48366
3.662
       11100
                        tick
                                  20517
                                                  # pic0=Dispatch0 br target,pic1=Re PC miss,sys
                                            19269 # pic0=Dispatch0_2nd_br,pic1=Dispatch0_mispred,sys
3.722
       11100
                        tick
                                  1838
3.812
       11100
                                  1781
                        tick
                                            21546 # pic0=Dispatch rs mispred,pic1=Re RAW miss,sys
3.912
       11100
                                 17800
                                          1243820 # pic0=Rstall storeQ,pic1=Rstall FP use,sys
                        tick
                                                  # pic0=Rstall_IU_use,pic1=Re_FPU_bypass,sys
4.022
       11100
                        tick
                                122989
                        +iar 128806/19
                                               53 # nich=Cucla ont nic1=DTT.R mice eve
```



ributed to

Application Monitoring-ripc2

Aggregated **gutrack**output

Ultra-III	ticks	sec	%		Measurements
DO IC miss DO br targ calc DO 2nd br DO mispred Drs mispred Rs storeQ Rs FP use Rs IU use Re FPU bypass Re RAW miss Re DC miss Re PC miss Re PC miss	2933194905 709057035	2.782 0.673 0.009 0.400 0.024	0.3% 0.1%		
DO_2nd_br	9375570	0.009	0.0%		of which processor
DU_mispred D rs misored	422139615 24932760	U. 4UU N. N24	0.0% 0.0%		
Rs_storeQ	83294492895	79.015 54.895	9.1%		events contributed t
Rs_FP_use	57868519605	54.895	6.3%		events continuated t
Rs_IU_use	9970661385	9.458 0.000	1.1% 0.0%		
Re RAW miss	2686694685	2.549	0.0%		stall
Re_DC_miss	464061620820	2.549 440.218 135.223	50.6%		
Re_EC_miss	142546870395	135.223	15.5%	(in DC miss)	time.
Re_PC_miss DTLB miss	74348460	0.000 5.995	0.0% 0.7%		
total	4470 74348460 628300315065	596.018	68.5%		
time instr IPC Grouping	142546870395 4470 74348460 628300315065 917205835095 505747594035 0.551 1.751				Stall times
unfinished fpop	0				Floating point traps
1					rtoating point traps
Ultra-III IC_ref IC_miss DC_rd DC_rd_miss DC_wr DC_wr DC_wr_miss EC_ref EC_misses	189100726920	0.206	100.0%	of IC ref	
DC rd	188104677270	0.000	100.0%	or ic_rer	
DC_rd_miss	8327843370	0.009	4.4%	of DC_rd	Events per instruction
DC_wr	63370469025	0.069	100.0%	of DO	Events per mstruction
DC_WI_MISS EC ref	236891795940	0.043	100.0%	or pc_wr	
		0.009	3.5%	of EC_ref	
EC_rd_miss	557599905	0.250 0.009 0.001 0.000 0.000	6.7%	of DC_rd_miss	
EC_ic_miss ITLB	16296120 2 9 400	0.000 0.000	23.9% N N%	of IC_miss of instructions	
FP inst A=	97990594365	M=10043949738	0 39.2	% of instructions	



System Monitoring-questat

System-wide version of cputrack

CPU counters

```
-c pic0=Instr cnt,pic1=Re DC miss,sys -c pic0=Dispatch0 IC miss,pic1=Re EC
# cpustat
  time cpu event
                         pīc0
          1 tick 2059035807 33974649 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
0 tick 1551600712 22778438 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
 5.009
 5.010
          0 tick 457169390 37188376 # pic0=Dispatch0_IC_miss.pic1=Re_EC_miss.sys
1 tick 328284013 41892660 # pic0=Dispatch0_IC_miss.pic1=Re_EC_miss.sys
10.009
10.010
15.009
             tick 1451190423 157834999 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
          O tick 1462169361 341406198 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
15.010
             tick 570276705 226545705 # pic0=Dispatch0_IC_miss,pic1=Re_EC_miss,sys
20.009
20.010
          O tick 586545226 126403413 # pic0=DispatchO IC miss.pic1=Re EC miss.sys
          O tick 1279091800 122489122 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
25.009
             tick 1850824519 363689893 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
25.010
             tick 493026173 128362677 # pic0=Dispatch0_IC_miss,pic1=Re_EC_miss,sys
30.009
30.010
          O tick 586294847 81941837 # picO=DispatchO IC miss,pic1=Re EC miss,sys
          0 tick 1946205173 229090921 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
35.009
             tick 1351275940 175492857 # pic0=Instr_cnt.pic1=Re_DC_miss.sys
35.010
40.009
             tick 555076554 74295003 # pic0=DispatchO IC miss, pic1=Re EC miss, sys
          0 tick 570543507 101949954 # pic0=Dispatch0_IC_miss,pic1=Re_EC_miss,sys
40.010
          0 tick 1881264848 286191421 # pic0=Instr_cnt,pic1=Re_DC_miss,sys
45.009
45.010
             tick 1318075599 133867092 # pic0=Instr cnt,pic1=Re DC miss,sys
             tick 577788523 111924098 # pic0=DispatchO IC_miss,pic1=Re_EC_miss,sys
50.009
             tick 646882743 155645759 # pic0=Dispatch0 IC miss, pic1=Re EC miss, sys
50.010
```



System Monitoring-questat

System-wide version of cputrack

Memory counters

```
cpustat -c MC reads 0, MC writes 0, sys -c MC reads 1, MC writes 1, sys -c MC reads
  time cpu event
                       pic0
                                  pīc1
 5.010
                     379284
                                435924 # pic0=MC reads_0,pic1=MC_writes_0,sys
         0 tick
 5.010
            tick
                                        # pic0=MC reads 0,pic1=MC writes 0,sys
10.010
            tick
                                        # pic0=MC_reads_1,pic1=MC_writes_1,sys
                      83775
         0 tick
                               2800104 # pic0=MC_reads_1,pic1=MC_writes_1,sys
10.010
                               2 # pic0=MC_reads_2,pic1=MC_writes_2,sys
480723 # pic0=MC_reads_2,pic1=MC_writes_2,sys
2909166 # pic0=MC_reads_3,pic1=MC_writes_3,sys
15.010
            tick
         0 tick
                     416247
15.010
            tick
                     179454
20.010
                                       # pic0=MC reads 3, pic1=MC writes 3, sys
20.010
            tick
25.010
                    2157225
            tick
                               1011898 # pic0=MC reads 0,pic1=MC writes 0,sys
            tick
25.010
                                      2 # pic0=MC_reads_0,pic1=MC_writes_0,sys
                               3055634 # pic0=MC_reads_1,pic1=MC_writes_1,sys
         0 tick
                     385880
30.010
                                       # pic0=MC reads_1,pic1=MC_writes_1,sys
30.010
            tick
                                      2 # pic0=MC reads 2, pic1=MC writes 2, sys
35.010
         1 tick
35.010
         0 tick
                     304115
                               426714 # pic0=MC_reads_2,pic1=MC_writes_2,sys
                               3392755 # pic0=MC_reads_3,pic1=MC_writes_3,sys
         0 tick
                     656979
40.010
            tick
                                        # pic0=MC_reads_3,pic1=MC_writes_3,sys
40.011
                    1668996
                                746562 # pic0=MC reads 0,pic1=MC writes 0,sys
45.010
            tick
45.010
            tick
                                        # pic0=MC_reads_0,pic1=MC_writes_0,sys
50.010
                                       # pic0=MC_reads_1,pic1=MC_writes_1,sys
            tick
50.010
            tick
                     738173
                               3366560 # pic0=MC reads 1,pic1=MC writes 1,sys
                                        # pic0=MC_reads_2,pic1=MC_writes_2,sys
55.010
            tick
                    1449829
                                728740 # pic0=MC_reads_2,pic1=MC_writes_2,sys
            tick
55.010
            tick
                                        # pic0=MC_reads_3,pic1=MC_writes_3,sys
60.010
                               3072477 # pic0=MC reads 3, pic1=MC writes 3, sys
60.012
            tick
                     891850
                                       # pic0=MC_reads_0,pic1=MC_writes_0,sys
65.010
             tick
                                575276 # pic0=MC_reads_0,pic1=MC_writes_0,sys
65.010
            tick
                    1042867
```



Application Monitoring-bw

Show memory bandwidth of application

- Based on cpustat
 - Read memory counters, massage output

```
nubbins% bw <target>
Read
      memory bandwidth: 1023.58642578125 MB/sec (total bytes = 17172930560)
Write memory bandwidth: 998.464149475098 MB/sec (total bytes = 16751448704)
Total memory bandwidth: 2022.05057525635 MB/sec (total bytes = 33924379264)
Elapsed time : 16 secs
```



System Monitoring-bastat Bus performance

# busstat -w pcis0							
time dev	event0	pic0	event1	pic1			
1 pcis0		200	dvma_stream_rd	200			
2 pcis0		98	dvma_stream_rd	98			
3 pcis0		197	dvma_stream_rd	197			
2 pcis0 3 pcis0 4 pcis0 5 pcis0 6 pcis0 7 pcis0		93	dvma_stream_rd	93			
5 pcis0		90	dvma_stream_rd	90			
6 pcis0		89	dvma_stream_rd	89			
7 pcis0		312	dvma_stream_rd	312			
8 pcis0		92	dvma_stream_rd	92			
9 pcis0		100	dvma_stream_rd	100			
10 pcis0		9204	dvma_stream_rd	9204			
11 pcis0		2688_	dvma_stream_rd	2688_			
12 pcis0		22237	dvma_stream_rd	22237			
13 pcis0		98	dvma_stream_rd	98			
14 pcis0		111	dvma_stream_rd	111			
15 pcis0 16 pcis0		116	dvma_stream_rd	116			
16 pcis0		104	dvma_stream_rd	104			
17 pcis0		515	dvma_stream_rd	515			
18 pcis0		1330	dvma_stream_rd	1330			
19 pcisO		1252	dvma_stream_rd	1252			
20 pcis0		1172	dvma_stream_rd	1172			
21 pcis0		189	dvma_stream_rd	189			
22 pcis0		100	dvma_stream_rd	100			
23 pcisO		90	dvma_stream_rd	90			
24 pcis0 25 pcis0		108	dvma_stream_rd	108			
25 pcis0		100	dvma_stream_rd	100			
26 pcis0	dvma stream rd	989	dvma stream rd	989			



HW Counter Library APIs

- Typical use by users
 - Read before and after block of code
 - Compute deltas
- API needs
 - Select counters, preset and read values
 - System call access
 - Direct user-mode reading?
 - Should be lower overhead than system call
- Profiling APIs
 - Specify counters, intervals for each
 - Usually for tool developers, not end users



HW-Counter Requirements, I

- Documented behavior
 - Actual behavior, not design intent or schematics
 - Verified behavior!
 - If they're not verified, they don't work
- Counters for all critical resources
 - Interesting events
 - Stall-cycle counts, not just event counts
 - Measures the cost of events
- Wide counter registers
 - Minimize need for OS to "widen" them to 64-bits
- As many registers as possible



HW-Counter Requirements, II

Counter contexts

- Counters virtualizable to user context
 - *i.e.*, Kernel save and restore on context switch
 - Overflow attributable to user context
- System-wide for system monitoring

CMT Issues

- Independent counter sets for each HW thread
- Counters for resource conflict among threads
- Measure number of active threads (binning?)

Wide-instruction chips

Counters for how many instructions in each cycle



HW-Counter Requirements, III

- Counter interface kernel driver
 - Read and write entire width of counter
 - Specify arbitrary interval for profiling
 - Specify arbitrary method for sampling



HW-Counter Requirements, IV

- Profiling-interrupt infrastructure
 - Easily attributable to specific counter
 - Delivered as precisely as feasible
 - *i.e.*, interrupt is synchronous to the context triggering it
 - If interrupt is deferred, allow SW to wait deterministically
 - Delivered with VA/PA (memory-related counters)
 - User needs to know which data objects are getting misses
- Instruction-sampling infrastructure
 - o *c.f.*, Profile-me
 - Detailed information on sampled instruction



HW-Counter Constraints, I

- Everything is a tradeoff ...
 - Complexity, alas, is somewhere
 - SW wants it in HW
 - HW wants in in SW
- Area constraints
 - Lead to pressure to reduce number of counters
 - But SW wants infinite number (approximately)
 - Lead to pressure to reduce width of counters
 - But SW prefers to never deal with rollover
 - But still need comparator to trigger profile interrupt
 - Are especially problematic for CMT



HW-Counter Constraints, II

- Routing constraints
 - Lead to delays due to long wires
 - Imply difficulty with counter placement
 - May make precise, synchronous delivery difficult
- Complex pipelines
 - Make precise, synchronous delivery difficult
- Mapping events to registers
 - SW wants any event to map to any register



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