A Hardware-Accelerated Steady-State Power Flow Solver

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Abstract:

Non-linear steady-state power flow solvers have typically relied on the Newton-Raphson method to efficiently compute solutions on General Purpose Processor (GPP)-based computer systems. Recently, high-performance computers have started to incorporate reconfigurable devices in their compute fabric, which can efficiently implement application-specific hardware. However, not all algorithms are suitable for a hardware-based implementation. For the steady-state power flow problem, we believe the Gauss-Seidel method is better suited to reconfigurable hardware.

We have implemented a prototype Gauss-Seidel solver on an SGI Altix 350 system equipped with a Virtex II 6000 FPGA. Our implementation was developed in a higher-level language (Celoxica's Handel-C) using a 32-bit fixed-point numerical representation. We developed our own CORDIC-based trigonometric and exponential functions, as well as our own fixed-point division operator and used vendor-provided libraries for the other operators. We were able to achieve a clock rate of 100 MHz for our implementation resulting in a speedup of 3.25 over a fixed-point software implementation and 4.25 over a floating-point software implementation, running on the 1.5 GHz Itanium 2 host processors of the Altix.

References:

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